

## ABSTRACT OF THE DISCLOSURE

The invention relates to a method for pinpointing erase-failed memory cells and to a relevant integrated non-volatile memory device, of the programmable and electrically erasable type comprising a sectored array of memory cells arranged in rows and columns, with at least one row-decoding circuit portion per sector being supplied positive and negative voltages. This method becomes operative upon a negative erase algorithm issue, and comprises the following steps: forcing the read condition of a sector that has not been completely erased; scanning the rows of said sector to check for the presence of a spurious current indicating a failed state; finding the failed row and electrically isolating it for re-addressing the same to a redundant row provided in the same sector.

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